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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/655,820	09/05/2003	Chan-ho Park	11948.9	7160

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KIRTON & McCONKIE
1800 Eagle Gate Tower
60 East South Temple Street
P.O. Box 45120
Salt Lake City, UT 84145-0120

EXAMINER	
HUYNH, ANDY	
ART UNIT	**PAPER NUMBER**
2818	

DATE MAILED: 10/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/655,820	PARK ET AL.	
	Examiner	Art Unit	
	Andy Huynh	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *02/27/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims **1-26** are pending in the application is acknowledged.

Priority

Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d) based on an application filed in REPUBLIC OF KOREA, 2002-53922 on 09/06/2002.

Information Disclosure Statement

This office acknowledges receipt of the following items from the applicant: Information Disclosure Statement (IDS) filed 02/27/2004. The references cited on the PTOL 1449 form have been considered.

Claim Objections

Claim **7** is objected to because of the following reasons: "an emitter region" should read – an emitter electrode--.

Claim Rejections - 35 U.S.C. § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims **1, 2, 4-11, 13, 15-18 and 20-26** are rejected under 35 U.S.C. 102(b) as being anticipated by Matthews (USP: 5,336,926).

Regarding claims **1 and 9**, Matthews discloses in Fig. 3 and the corresponding texts as set forth in column 3, line 30-column 4, line 14, a bipolar transistor comprises:

a first collector region/a buried layer (12) of a first conductive type having high impurity concentration (N+);

a second collector region/an epitaxial layer (11) of a first conductive type having high impurity concentration (N^-), the second collection region/the epitaxial layer formed on the first collector region/the buried layer;

a base region (17, 18) of a second conductive type (P) being formed a predetermined portion of the second collector region/the epitaxial layer; and

an emitter region (20) of a first conductive type (N+) being formed in the base region;

wherein a third collector region/a localized region (15) is further formed at an interface between the base region and the second collector region, the third collector region whose impurity concentration (N+) is higher than that of the second collector region (N^-).

Regarding claim **2**, Matthews discloses in Fig. 3 the bipolar transistor wherein the impurity concentration of the third collector region/the localized region gradually decreases, as the third collector region/the localized region more closely approaches an interface between the third collector region/the localized region and the base region to the second collector region/the epitaxial layer.

Regarding claims **4-6**, Matthews discloses the bipolar transistor wherein the second collector region/the epitaxial layer has impurity concentration of approximately $10^{16}/cm^3$ and the first collector region/the buried layer has higher impurity concentration than the second collector region/the epitaxial layer (col. 3, lines 35-38); and wherein the third collector region/the localized region has impurity concentration of approximately $10^{16}/cm^3$ (col. 4, lines 32-33).

Regarding claims **7 and 20**, Matthews discloses in Fig. 3 the bipolar transistor further comprising:

a base electrode (BASE) being formed in a predetermined portion of the base region so as to contact the base region;

an emitter electrode (EMITTER) being formed in a predetermined portion of the emitter region so as to contact the emitter region; and

it is inhering that a collector electrode (not shown) being formed at the bottom of the first collector region.

Regarding claim **8**, Matthews discloses in Fig. 3 the bipolar transistor wherein the impurity concentrations of the base region, the emitter region, and the first collector region gradually increase toward an interface between the base region and the base electrode, an interface between the emitter region and the emitter electrode, and an interface between the collector region and the collector electrode, respectively.

Regarding claims **10 and 16**, Matthews discloses the bipolar transistor wherein impurities of the first conductive type are phosphorous ions and impurities of the second conductive type are boron ions (col. 9, lines 63-65).

Regarding claims **11 and 15**, Matthews discloses in Fig. 3 and the corresponding texts as set forth in column 3, line 30-column 4, line 14, a method of manufacturing a bipolar transistor, comprises:

forming a high-concentration first collector region/a buried layer (12) of a first conductive type (N+) at the bottom of a semiconductor substrate that is doped with low-concentration impurities of a first conductive type (N^-), thereby defining a second collector region/an epitaxial layer (11) on the semiconductor substrate on the first collector region/the buried layer;

implanting at least one of first conductive impurities (N) for a third collector region/a localized region (15) and second conductive impurities (P) for a base region (17, 18) into the second collector region/the epitaxial layer;

activating the first conductive impurities for the third collector region/the localized region and the second conductive impurities for the base region, thereby forming the base region and the third collector region/the localized region below the base region; and

forming an emitter region (20) in the base region,

wherein the third collector region/the localized region has higher impurity concentration than the second collector region/the epitaxial layer.

Regarding claim **13**, Matthews discloses in Fig. 3 the method wherein the first collector region/the buried layer and the emitter region are obtained by ion-implanting corresponding impurities into the first collector region/the buried layer and the emitter region and activating the implanted impurities, respectively.

Regarding claims **17 and 21**, Matthews discloses in Fig. 3 and the corresponding texts as set forth in column 3, line 30-column 4, line 14, a bipolar transistor comprises:

a first collector region/a buried layer (12) having a first concentration of a first conductive type (N+);

a second collector region/an epitaxial layer (11) having a second concentration of a first conductive type (N^-) and formed on the first collector region;

a third collector region/a localized region (15) having a third concentration of a first conductive type (N+) and formed on the second collector region/the epitaxial layer, wherein the third concentration is higher than the second concentration;

a base region (17, 18) formed on a portion of the third collector region/the localized region; and

an emitter region (20) formed on a portion of the base region.

Regarding claim 18, Matthews discloses in Fig. 3 the bipolar transistor wherein the third concentration decreases from the base region to the second collector region.

Regarding claims **22 and 23**, Matthews discloses in Fig. 3 and the corresponding texts as set forth in column 3, line 30-column 4, line 14, a collector for a bipolar transistor comprises:

a first collector region/a buried layer (12) having a first impurity concentration of a first conductive type (N+);

a second collector region/an epitaxial layer (11) having a second impurity concentration of a first conductive type (N^-) and formed on the first collector region/the buried layer;

a third collector region/a localized region (15) having a third impurity concentration of a first conductive type (N+) and formed on the second collector region/the epitaxial layer, wherein the third impurity concentration is higher than the second impurity concentration; and

wherein the third concentration decreases from the base region to the second collector region.

Regarding claims **24 and 25**, Matthews discloses in Fig. 3 and the corresponding texts as set forth in column 3, line 30-column 4, line 14, a method for making a bipolar transistor, the method comprises:

providing a first collector region/a buried layer (12) having a first concentration of a first conductive type (N+);

providing a second collector region/an epitaxial layer (11) having a second concentration of a first conductive type (N^-) and formed on the first collector region/the buried layer;

providing a third collector region/a localized region (15) having a third concentration of a first conductive type (N+) and formed on the second collector region/the epitaxial layer, wherein the third concentration is higher than the second concentration;

providing a base region (17, 18) formed on a portion of the third collector region/the localized region;

providing an emitter region (20) formed on a portion of the base region;

wherein the third concentration decreases from the base region to the second collector region.

Regarding claim **26**, Matthews discloses in Fig. 3 and the corresponding texts as set forth in column 3, line 30-column 4, line 14, a method for making a collector of bipolar transistor, the method comprises:

providing a first collector region/a buried layer (12) having a first concentration of a first conductive type (N+);

providing a second collector region/an epitaxial layer (11) having a second concentration of a first conductive type (N$^-$) and formed on the first collector region/the buried layer; and

providing a third collector region/a localized region (15) having a third concentration of a first conductive type (N+) and formed on the second collector region/the epitaxial layer, wherein the third concentration is higher than the second concentration.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims **3, 12 and 19** are rejected under 35 U.S.C. 103(a) as being unpatentable over Matthews (USP: 5,336,926) in view of Yukimoto (USP: 4,337,474).

Matthews discloses the claimed limitations except for the bipolar transistor wherein the third collector region has lower impurity concentration than the first collector region. Yukimoto teaches in Fig. 7 and the corresponding texts as set forth in column 6, lines 30-42, the bipolar transistor comprising the third collector region (22, N) has lower impurity concentration than the first collector region (10, N+). It would have been obvious to one of ordinary skill in the art at

the time of the invention was made to incorporate the teaching of the bipolar transistor comprising the third collector region has lower impurity concentration than the first collector region, as taught by Yukimoto into Matthews' structure to form the claimed limitation in order to improve the device having a high operating current and a high output while having good high frequency characteristics (col. 7, lines 28-30).

Claim **14** is rejected under 35 U.S.C. 103(a) as being unpatentable over Matthews (USP: 5,336,926) in view of FIG.1 (PRIOR ART), Applicant's admitted prior art (AAPA).

Matthews discloses the claimed limitations except for the method after forming the emitter region, further comprises depositing an insulating layer on the semiconductor substrate on which the base region and the emitter region are formed; partially etching the insulating layer to expose predetermined portions of the base region and the emitter region; forming a base electrode and an emitter electrode on the exposed portions of the based region and the emitter region; and forming a collector electrode at the first collector region. FIG.1 (PRIOR ART) teaches that the method after forming the emitter region, further comprises depositing an insulating layer on the semiconductor substrate on which the base region and the emitter region are formed; partially etching the insulating layer to expose predetermined portions of the base region and the emitter region; forming a base electrode and an emitter electrode on the exposed portions of the based region and the emitter region; and forming a collector electrode at the first collector region. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to utilize the teaching of FIG.1 (PRIOR ART) to incorporate into and to modify Matthews' structure to arrive the claim limitations, since such a modification would have involved only routine skill in the art.

Conclusion

A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andy Huynh, (571) 272-1781. The examiner can normally be reached on Monday-Friday from 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The Fax number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the -status of this application or proceeding should be directed to the receptionist whose phone number is (703) 308-0956.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ah

Andy Huynh

10/24/04

Patent Examiner